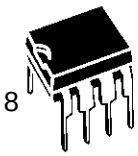
SGS-THOMSON MICROELECTRONICS

ST95P02

SERIAL ACCESS SPI BUS 2K (256 x 8) EEPROM

DATA BRIEFING

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 3V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- ***The ST95P02 will be replaced shortly by the updated version ST95020***



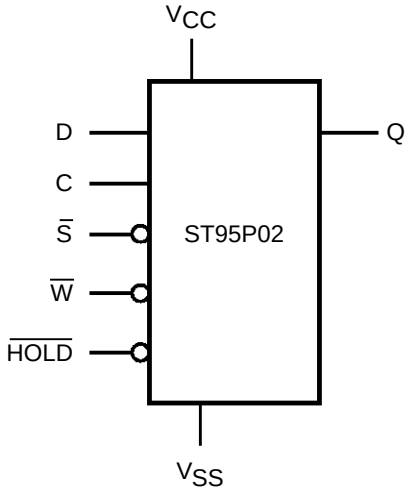
PSDIP8 (B)
0.25mm Frame

SO8 (M)

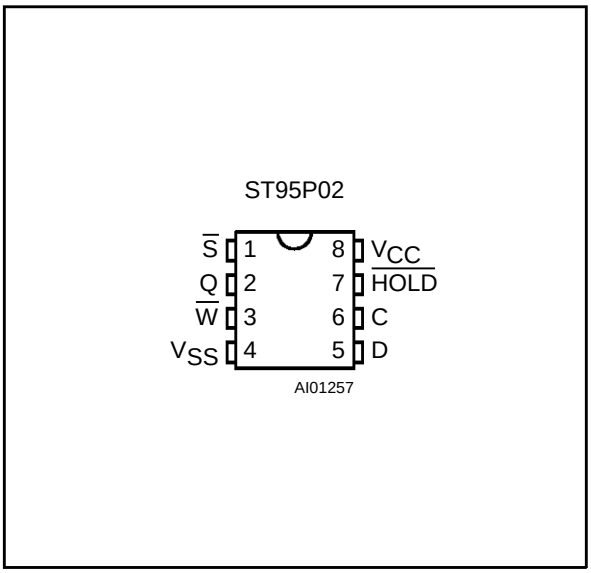
DESCRIPTION

The ST95P02 is a 2K bit Electrically Erasable Programmable Memory (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The 2K bit memory is organised as 16 pages of 16 bytes. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q). The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$). The write operation is disabled by a write protect input ($\overline{W}$).

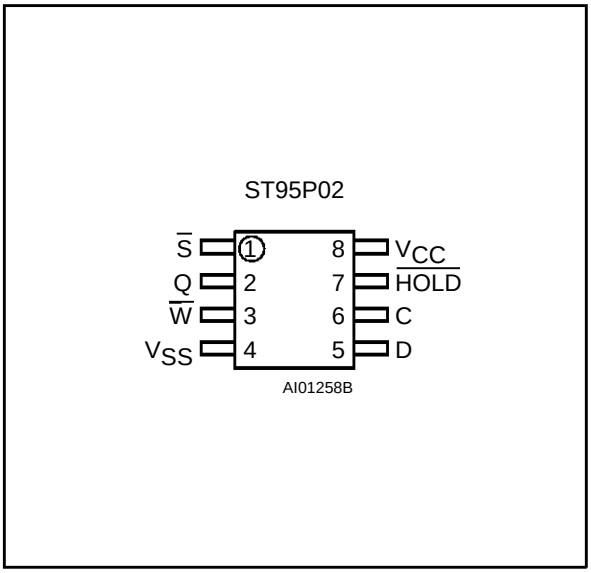
Logic Diagram



DIP Pin Connections



SO Pin Connections



Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Ordering Information Scheme

For a list of available options refer to the current Memory Shortform catalogue.
For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.

Example: ST95P02 M 6 TR

Data Strobe

P (1) D ⌐ Q ¬

Package

B PSDIP8
0.25mm Frame

M SO8
150mil Width

Temp. Range

1 0 to 70 °C

6 –40 to 85 °C

3 –40 to 125 °C

Option

TR Tape & Reel
Packing

Note: 1. Data In strobed on rising edge of the clock (C) and Data Out synchronized from the falling edge of the clock.